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LETTERS

Enhancing semiconductor device performance using ordered dopant arrays

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As the size of semiconductor devices continues to shrink, the normally random distribution of the individual dopant atoms within the semiconductor becomes a critical factor in determining device performance—homogeneity can no longer be assumed[1–5]. Here we report the fabrication of semiconductor devices in which both the number and position of the dopant atoms are precisely controlled. To achieve this, we make use of a recently developed single-ion implantation technique[6–9], which enables us to implant dopant ions one-by-one into a fine semiconductor region until the desired number is reached. Electrical measurements of the resulting transistors reveal that device-to-device fluctuations in the threshold voltage (V_{th}; the turn-on voltage of the device) are less for those structures with ordered dopant arrays than for those with conventional random doping. We also find that the devices with ordered dopant arrays exhibit a shift in V_{th}, relative to the undoped semiconductor, that is twice that for a random dopant distribution (−0.4 V versus −0.2 V); we attribute this to the uniformity of electrostatic potential in the conducting channel region due to the ordered distribution of dopant atoms. Our results therefore serve to highlight the improvements in device performance that can be achieved through atomic-scale control of the doping process. Furthermore, ordered dopant arrays of this type may enhance the prospects for realizing silicon-based solid-state quantum computers[10].

Doping of impurity atoms into semiconductors is essential to achieving the proper function of semiconductor devices through the control of electrical characteristics[11]. So far, the semiconductor has been assumed to be homogeneously doped in the active channel region. In nanoscale semiconductor devices, however, the channel region will contain few dopant atoms and the assumption of uniform dopant distribution is no longer feasible. In this situation, the statistical fluctuation in dopant atom number due to a random Poisson distribution causes serious fluctuation in the device's functioning.

In order to suppress the conductance fluctuation due to the fluctuation in the number of dopant atoms, we have previously attempted to tailor the conductance of submicrometre resistors, which corresponds to the channel region in semiconductor devices, by one-by-one implantation of dopant ions, which we refer to as single ion implantation (SII). In SII, single ions are extracted by chopping a focused ion beam using a small aperture and high frequency beam deflection, and the number of implanted ions is controlled one-by-one by detecting secondary electrons emitted from a target outside upon a single ion incidence. A broad range of ion species such as Be, B, Si, P, Fe, Co, Ni, Cu, Ga, Ge, As, Pd, In, Sb, Pt and Au can now be implanted one-by-one with an aiming precision of 60 nm (ref. 9) and with potentially higher accuracy by remodelling the focused ion beam optics for SII. The number of single ions necessary to tailor the conductance value to a certain value on the higher side of the initial distribution was implanted in each resistor. The initial conductance fluctuation (the ratio of the standard deviation to the average value of conductance from 22 resistors) of 63% was reduced to only 13% (ref. 8). By analysing the origin of the fluctuation after SII, the residual fluctuation turned out to be the fluctuation in the dopant atom position. Thus we have found that the control of not only the dopant atom number but also its position is essential.

We note that a solid-state quantum computer has been proposed by Kane[10]. Kane's original proposal requires single phosphorus atoms to be placed in an array in a Si layer beneath an insulating oxide layer. However, the incorporation of the dopant array is a major problem that has yet to be overcome. In this Letter, we demonstrate the fabrication of a semiconductor with an ordered array of dopant atoms.

Figure 1a sketches a simplified version of the resistor. The channel size is 300 nm wide, 3.2 μm long and 90 nm thick employing a phosphorus-doped n-type (100) silicon-on-insulator (SOI) substrate (resistivity 8–12 ohm cm) patterned using standard photolithography. A 25 nm silicon dioxide layer covers the channel region to passivate the surface states, which act as carrier generation-recombination centres. The devices have a simple back-gated device configuration on a silicon substrate, where underlying buried oxide was used as the back gate. The drain current (I_d) from the source to the drain is controlled by the gate voltage (V_g) from the substrate through the buried oxide of 90 nm thickness. The electrodes attached along with the channel (Fig. 1b) for measuring the semiconductor resistivity by the four point probe technique were not employed in this work. Figure 1c shows an atomic force microscope (AFM) image of single-ion incident sites in a fission track detector, fabricated by SII.

Typical electrical characteristics (Fig. 2) show that I_d increases as source-to-drain voltage (V_d) increases at a positive back-gate bias, and saturates beyond the pinch-off point. Figure 2a confirms that our device is based on the standard field-effect transistor (FET) theory, and that the Fermi level in the channel is controlled by the back-gate and drain bias. The device exhibits an accumulation-mode n-channel transistor behaviour. In advance of SII, the initial threshold voltage (V_{th}^{i}) was evaluated by the extrapolation of the linear part of the curve to the V_g axis in the V_g dependence of I_d under a certain V_d of 0.1 V (Fig. 2b). The measurement was carried out at room temperature by using a semiconductor parameter analyser (Keithley 4200-SCS) and in a vacuum to avoid the disturbance caused by adsorbates.

Doubly charged P single ions were implanted one-by-one at 30 kV into the channel region at a centre-to-centre distance (pitch) of 100 nm through the 25-nm-thick surface oxide by SII, as shown in Fig. 3a, where a part of the channel region (0.3 μm × 3.2 μm) is indicated. The number of implanted ions in the channel was set to be 96. The projected range and the projected range straggling were calculated to be 86 nm and 22 nm, respectively, by using Monte Carlo code SRIM2003 (http://www.SRIM.org). For comparison with the ordered array, samples with random doping were also prepared by implanting P ions at an interval of 300 nm under the condition that the aiming precision was intentionally lowered down to 170 nm (Fig. 3b). The number of ions was set to be exactly the same as that of the ordered doping. The implanted samples were then lamp-annealed at a temperature of 900 °C for 3 min in N_2 to electrically activate the implanted ions. V_{th} measurement was carried out under the same condition as the initial V_{th} measurement and the difference between V_{th} before and after the SII was evaluated.

The V_{th} shift of our devices is now derived by using standard FET equations. The V_d dependence of I_d in a device with channel length L, width W and thickness t_{SOI} in the low-bias linear region is deduced as $I_d = (Wt_{SOI}/L)\mu_n C_T(V_g - V_{th})V_d$, where $V_{th} = (1/C_T)(Q_{it} - qN_D - qN_D^{i}) = V_{th}^{i} - qN_D/C_T$. Here μ is the mobility, q the elementary charge, N_D^{i} the initial dopant concentration, N_D the concentration of implanted ions, C_T the total capacitance per unit area, and Q_{it} the Si/SiO$_2$ interface-trapped charges. V_{th} monotonically decreases as the number of implanted ions increases. We define the difference between the V_{th} shift (ΔV_{th}) before and after single ion implantation as $\Delta V_{th} = V_{th} - V_{th}^{i} = -qN_D/C_T$. ΔV_{th} is directly proportional to the number of newly added dopants, and hence is a good means of counting the number of added dopants. By assessing ΔV_{th}, we eliminate the fluctuations unintentionally incorporated during the device fabrication processes, such as the fluctuation in initial dopant distribution, lithographical channel size and film thickness.

Figure 4 shows the histograms of ΔV_{th} distribution obtained from 10 FETs with ordered channel doping and 10 FETs with random channel doping. The ΔV_{th} distribution of FETs with the ordered dopant array (Fig. 4a) is much narrower than that of FETs with random channel doping (Fig. 4b). The ΔV_{th} values of FETs with random implantation deviated considerably from the mean value (Fig. 4b); the fluctuation in the dopant atom position from one device to another explains this dispersion. Gaussian fitting in the ordered dopant distribution shows a standard deviation of only 0.1 V, which is three times smaller than the random dopant distribution. We attribute the reduction of V_{th} fluctuation to the precise control of both dopant atom number and position. In addition, we find a pronounced difference in that the average value of ΔV_{th} (−0.4 V) for the ordered dopants is two times lower than that (−0.2 V) of the FETs with the random distribution of dopants, even though the dopant number is exactly same for both FETs. The larger negative ΔV_{th} for the ordered distribution indicates that the channel is open under the lower gate voltage.

The theoretical value of ΔV_{th} is calculated by using equation

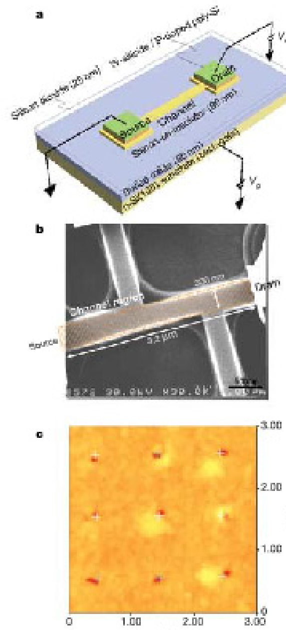

Figure 1 | Experimental device and results of single ion implantation. **a**, Illustration of device structure for controlling V_{th} through the control of dopant atom number and position by single ion implantation (SII). The oxide film (which is not displayed) covers the channel region to passivate the surface states. The current from source to drain is controlled by the gate voltage (V_g) from the back through the buried oxide. V_d, drain voltage. **b**, A scanning electron microscope (SEM) image of a representative device. The feature size is 300 nm wide, 3.2 μm long and 90 nm thick. Black scale bar at bottom right, 500 nm. **c**, Typical atomic force microscope (AFM) image of etch-pits created in a fission track detector by single ions. The white crosses indicate the aimed positions.

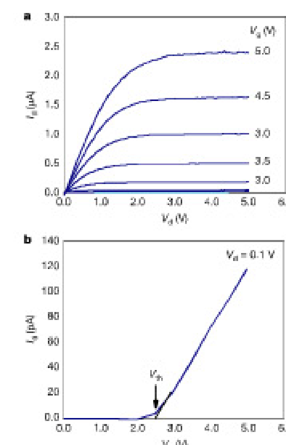

Figure 2 | Typical electrical characteristics. **a**, Drain current (I_d) versus drain voltage (V_d) characteristic at increasing gate voltage (V_g) in steps of 0.5 V starting from 0 V and going up to 5 V. The data indicate the standard electric field effect transistor (FET) behaviour. **b**, V_g dependence of I_d at a grounded source and a small drain potential of 0.1 V. Linear extrapolation gives a threshold voltage (V_{th}).

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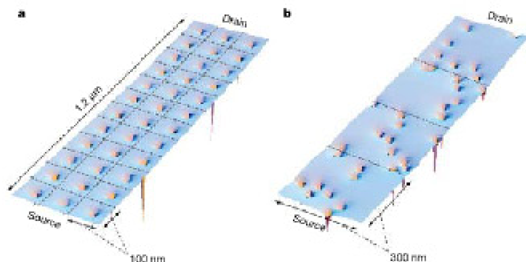

Figure 3 | Calculated potential distribution of the channel region. **a**, Potential distribution of the ordered dopant array. The energy is measured upwards. Phosphorus single ions were implanted at a pitch of 100 nm by SII. **b**, Potential distribution of the conventional random distribution of dopant atoms, made by implanting ions at an interval of 300 nm under the condition of a lowered aiming accuracy of 170 nm, shown for comparison.

$\Delta V_{th} = -qN_D/C_T$, in which the individual dopant distribution is, a *priori*, not taken into account. The total capacitance of our sample is expressed as a series combination of the buried oxide capacitance (C_{BOX}) and the semiconductor substrate capacitance (C_s), and calculated to be $C_T = C_sC_{BOX}/(C_s + C_{BOX}) = 6.7 \times 10^{-17}$ F.

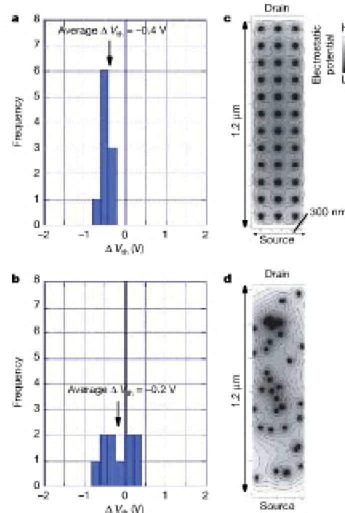

Figure 4 | Histograms of V_{th} shift (ΔV_{th}) before and after single-ion implantation from 10 resistors. **a**, Ordered dopant distribution. **b**, Conventional random dopant distribution. Gaussian fitting (curve) in the ordered dopant distribution shows a standard deviation of only 0.1 V, which is three times smaller than the random dopant distribution. **c**, **d**, The contour map of the Coulomb potential in the channel with ordered (**c**) and random (**d**) dopant distribution.

When 96 ions are implanted, the ΔV_{th} is calculated to be −0.2 V, and this value coincides with the average ΔV_{th} obtained in random channel doping. The larger negative shift of ΔV_{th} (−0.4 V) in the ordered sample cannot be explained by the conventional model, where the discrete nature of the dopant atom is ignored. To understand the larger negative shift of ΔV_{th} from the viewpoint of the discrete dopant model, we calculate the distribution of Coulomb potentials produced by ionized dopant atoms in the channel region. Figure 4 exhibits the contour map of Coulomb potentials. Here no bias is applied to the source-to-drain and the gate electrode. The potential is assumed to be Coulombic, $q^2/(4\pi\varepsilon_s r)$, without the screening effect by mobile carriers and the electron energy is measured upwards (here ε_s and r represent respectively semiconductor permittivity and distance from the centre of the atom).

The lighter regions in Fig. 4c and d correspond to the potential barrier for electrons injected from the source. When we apply a positive voltage to the gate at a particular drain voltage, a conductive path is formed from source to drain in the channel region at a certain gate voltage, which corresponds to the threshold voltage of the device. The ordered dopant array forms a homogeneous potential distribution in the channel, as shown in Fig. 4c, resulting in the formation of a uniform current path.

In Fig. 4d, dopant atoms are randomly located within the channel region, so there is considerable variance in electrostatic potential at any point in the device. The current in the presence of potential fluctuations percolates through the 'valleys' in the potential landscape. The location and magnitude of the potential 'valleys' will strongly depend on the arrangement of the dopant ions. The current path through the channel region differs from device to device, leading to deviation in V_{th}. In the random channel doping, some parts of the channel have already reached the conductive state (darker areas), whereas others are still in the non-conductive state (lighter areas). Thus, the remaining non-conductive regions are due to the nonhomogeneous potential block in the current path formation.

As shown in Fig. 4c, the uniform channel potential in the ordered sample is obviously lower than that in the random sample (Fig. 4d). We conclude that the uniformity of channel potential lowers the voltage required to open the channel from source to drain, which allows for early turn-on in parts of the channel and results in the lower threshold voltage. Thus marked improvements in device properties could be obtained for future semiconductor electronics if dopant distributions could be precisely controlled. How a similar scheme could be implemented in mass production remains an open question.

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